

IN THE CLAIMS

1. (Currently Amended) A programmable delay cell comprising:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

[[two]]three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the [[two]]three or more pass gates is coupled to the conductor and a second terminal of the each of the [[two]]three or more pass gates is coupled to the capacitor, wherein [[an]]impedance of each of said pass gates is to be controlled by an independent ~~respective~~ control signal, such that combined impedance of said pass gates is controlled by at least three control signals.

2. (Canceled)

3. (Original) The programmable delay cell of claim 1, further comprising:

a variable impedance transistor coupled to a high supply rail and to said conductor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

4. (Currently Amended) A programmable delay cell comprising:

a conductor coupled to an output of said programmable delay cell;

a switch transistor coupled to the conductor;

three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to a capacitor coupled to a low supply rail; and

a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch terminal and the variable impedance transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

5. (Original) The programmable delay cell of claim 4, wherein said control signal is set in response to output from a system to measure changes in the behavior of an integrated circuit comprising said programmable delay cell, said changes resulting, at least in part, from variations in a supply voltage to said integrated circuit, variations in an ambient temperature and variations in a temperature of said integrated circuit.

6. (Original) The programmable delay cell of claim 4, wherein said control signal is a continuous signal.

7. (Currently Amended) A controller comprising:

an output buffer to generate an electrical signal on a conductor coupled to said controller; and

a programmable delay cell coupled to said output buffer, wherein said programmable delay cell includes at least:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

[[two]]~~three~~ or more pass gates coupled in parallel to each other, wherein a

first terminal of each of the ~~two or more~~three or more pass gates is

coupled to the conductor and a second terminal of the each of the ~~two~~

~~or more~~three or more pass gates is coupled to the capacitor, wherein

[[an]] impedance of each of said pass gates is to be controlled by an

independent ~~respective~~ control signal, such that combined impedance of said pass gates is controlled by at least three control signals.

8. (Original) The controller of claim 7, further comprising:

a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

9. (Original) The controller of claim 8, further comprising:

a memory to store one or more values to program to said register.

10. (Original) The controller of claim 7, wherein said controller is a memory controller.

11. (Original) The controller of claim 7, further comprising:

one or two registers coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer.

12. (Currently Amended) A controller comprising:

an output buffer to generate an electrical signal on a conductor coupled to said controller; and

a programmable delay cell coupled to said output buffer, wherein said programmable delay cell includes at least:

a conductor coupled to an output of said programmable delay cell;

a switch transistor coupled to the conductor;

three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the

conductor and a second terminal of the each of the three or more pass gates is coupled to a capacitor coupled to a low supply rail; and
a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch terminal and the variable impedance transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

13. (Original) The controller of claim 12, wherein said control signal is set in response to output from a system to measure changes in the behavior of said controller, said changes resulting, at least in part, from variations in a supply voltage to said controller, variations in an ambient temperature and variations in a temperature of said controller.

14. (Original) The controller of claim 12, further comprising:
a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

15. (Original) The controller of claim 14, further comprising:
a memory to store one or more values to program to said register.

16. (Original) The controller of claim 12, wherein said controller is a memory controller.

17. (Original) The controller of claim 12, further comprising:
one or two registers coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer.

18. (Currently Amended) A controller comprising:

an input buffer to receive an electrical signal from a conductor coupled to said controller; and

a programmable delay cell coupled to said input buffer, wherein said programmable delay cell includes at least:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

[[two]]~~three~~ or more pass gates coupled in parallel to each other, wherein a first terminal of each of the ~~two or more~~three or more pass gates is coupled to the conductor and a second terminal of each of the ~~two or more~~three or more pass gates is coupled to the capacitor, wherein [[an]]impedance of each of said pass gates is to be controlled by an independent respective control signal, such that combined impedance of said pass gates is controlled by at least three control signals.

19. (Original) The controller of claim 18, further comprising:

a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

20. (Original) The controller of claim 19, further comprising:

a memory to store one or more values to program to said register.

21. (Original) The controller of claim 18, wherein said controller is a memory controller.

22. (Currently Amended) A controller comprising:

an input buffer to receive an electrical signal from a conductor coupled to said controller; and

a programmable delay cell coupled to said input buffer, wherein said programmable delay cell includes at least:

- a conductor coupled to an output of said programmable delay cell;
- a switch transistor coupled to the conductor;
- three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to a capacitor coupled to a low supply rail; and

a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch transistor and the variable impedance transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

23. (Original) The controller of claim 22, wherein said control signal is set in response to output from a system to measure changes in the behavior of said controller, said changes resulting, at least in part, from variations in a supply voltage to said controller, variations in an ambient temperature and variations in a temperature of said controller.

24. (Original) The controller of claim 22, further comprising:

- a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

25. (Original) The controller of claim 24, further comprising:

a memory to store one or more values to program to said register.

26. (Original) The controller of claim 22, wherein said controller is a memory controller.

27. (Withdrawn) A printed circuit board comprising:

- a graphics chip;

- a controller including at least:

- an output buffer to generate an electrical signal on a conductor coupled to said controller;

- a programmable delay cell connected to said output buffer to directly provide input to said output buffer; and

- a register coupled to said programmable delay cell to store an output-window-centering value that determines a time delay of said input relative to input to said programmable delay cell; and

- a memory having programmed therein output-window-centering values for one or more configurations of devices to be installed on said printed circuit board and coupled to said controller.

28. (Withdrawn) The printed circuit board of claim 27, wherein said controller is a memory controller.

29. (Withdrawn) The printed circuit board of claim 28, further comprising:

- one or more memory devices coupled to said memory controller, and wherein said memory controller is to drive said electrical signal to one or more of said one or more memory devices via said conductor.

30. (Withdrawn) The printed circuit board of claim 27, wherein said controller further includes:

one or two registers coupled to said output buffer to store a source-driving-impedance value that determines the source driving impedance of said output buffer and to store a sink-driving-impedance value that determines the sink driving impedance of said output buffer.

31. (Withdrawn) A printed circuit board comprising:

a graphics chip;

a controller including at least:

an input buffer to receive an electrical signal from a conductor coupled to said controller; and

a programmable delay cell connected to said input buffer to directly receive output of said input buffer; and

a register coupled to said programmable delay cell to store an input-window-centering value that determines a time delay of output of said programmable delay cell relative to said output of said input buffer; and

a memory having programmed therein input-window-centering values for one or more configurations of devices to be installed on said printed circuit board and coupled to said controller.

32. (Withdrawn) The printed circuit board of claim 31, wherein said controller is a memory controller.

33. (Withdrawn) The printed circuit board of claim 32, further comprising:

one or more memory devices coupled to said memory controller, and wherein one or more of said memory devices is to drive said electrical signal to said memory controller via said conductor.

34. (Currently Amended) A printed circuit board comprising:

a graphics chip;

a controller including at least a programmable delay cell, said programmable delay cell including at least:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

~~two or more~~three or more pass gates coupled in parallel to each other, wherein

a first terminal of each of the ~~two or more~~three or more pass gates is coupled to the conductor and a second terminal of each of the ~~two or more~~three or more pass gates is coupled to the capacitor, wherein [[an]] impedance of each of said pass gates is to be controlled by an independent ~~respective~~ control signal, such that combined impedance of said pass gates is controlled by at least three control signals.

35. (Canceled)

36. (Original) The printed circuit board of claim 34, wherein said programmable delay cell further includes:

a variable impedance transistor coupled to a high supply rail and to said conductor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

37. (Withdrawn) A printed circuit board comprising:

a graphics chip;

a controller including at least a programmable delay cell, said programmable delay cell including at least:

a conductor coupled to an output of said programmable delay cell; and

a variable impedance transistor coupled to a high supply rail and to said conductor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

38. (Withdrawn) The printed circuit board of claim 37, wherein said control signal is set in response to output from a system to measure changes in the behavior of said controller, said changes resulting, at least in part, from variations in a supply voltage to said controller, variations in an ambient temperature and variations in a temperature of said controller.

39. (Withdrawn) The printed circuit board of claim 37, wherein said control signal is a continuous signal.

40. (Withdrawn) A computer apparatus comprising:

an audio input device; and

a printed circuit board comprising:

a memory controller including at least:

output-delay control registers to store output-window-centering values affecting time delays introduced by first programmable delay cells directly into inputs of output buffers of said memory controller; and

input-delay control registers to store input-window-centering values affecting time delays introduced by second programmable delay cells directly into outputs of data input buffers of said memory controller; and

a basic input/output system device having programmed therein output-window-centering values and input-window-centering values for one or more configurations of memory devices to be installed on said printed circuit board and coupled to said memory controller.

41. (Withdrawn) The apparatus of claim 40, wherein said memory controller further includes:
driving impedance control registers to store source-driving-impedance values and
sink-driving-impedance values for said output buffers.

42. (Withdrawn) The apparatus of claim 41, wherein said basic input/output system device has programmed therein source-driving-impedance values and sink-driving-impedance values for said one or more configurations of memory devices.

43. (Withdrawn) A method comprising:
determining a time delay introduced by a programmable delay cell into a signal by
controlling impedances of pass gates internal to said programmable delay cell.

44. (Withdrawn) The method of claim 43, further comprising:
adjusting said time delay by controlling a variable impedance of a variable impedance transistor internal to said programmable delay cell.

45. (Withdrawn) The method of claim 44, wherein controlling said variable impedance includes at least controlling said variable impedance in response to output from a system to measure changes in the behavior of an integrated circuit comprising said programmable delay cell, said changes resulting, at least in part, from variations in a supply voltage to said integrated circuit, variations in an ambient temperature and variations in a temperature of said integrated circuit.

46. (Withdrawn) A method comprising:

determining a time delay introduced by a programmable delay cell into a signal by
controlling a variable impedance of a variable impedance transistor internal to
said programmable delay cell.

47. (Withdrawn) The method of claim 46, further comprising:

adjusting said time delay by controlling impedances of pass gates internal to said
programmable delay cell.

48. (Withdrawn) The method of claim 46, wherein controlling said variable impedance
includes at least controlling said variable impedance in response to output from a system to
measure changes in the behavior of an integrated circuit comprising said programmable delay
cell, said changes resulting, at least in part, from variations in a supply voltage to said
integrated circuit, variations in an ambient temperature and variations in a temperature of said
integrated circuit.

49. (Withdrawn) A method comprising:

for one or more configurations of devices to be installed on printed circuit boards,
determining values to be programmed to registers of controllers to be installed
on said printed circuit boards,
where said registers affect timing of signals between said controllers and said devices
once said controllers and said devices are installed on said printed circuit
boards by affecting one or more of the following: driving impedances of output
buffers of said controllers, time delays introduced by first programmable delay
cells directly into inputs of said output buffers and time delays introduced by

second programmable delay cells directly into outputs of input buffers of said controllers.

50. (Withdrawn) The method of claim 49, further comprising:

storing said values in memories to be installed on said printed circuit boards.

51. (Withdrawn) The method of claim 49, further comprising:

determining calibrated values to be programmed to said registers based on timing of signals between said controllers and said devices once said controllers and said devices are installed on a particular type of printed circuit board; and
storing said calibrated values in memories to be installed on said particular type of printed circuit board.

52. (Withdrawn) A method comprising:

programming digital values to registers of a controller, said digital values retrieved from a memory based on configuration information regarding one or more devices,

wherein said registers affect timing of signals between said controller and said devices by affecting one or more of the following: time delays introduced by first programmable delay cells directly into inputs of output buffers of said controller and time delays introduced by second programmable delay cells directly into outputs of input buffers of said controller.

53. (Withdrawn) The method of claim 52, further comprising:

bringing said controller and said devices to operation conditions; and
performing one or more tests that said signals are accurately received.

54. (Withdrawn) The method of claim 53, wherein said one or more tests test violations of setup time restrictions and hold time restrictions of input channels of said devices.

55. (Withdrawn) The method of claim 53, wherein said one or more tests test violations of setup time restrictions and hold time restrictions of input channels of said controller.

56. (Withdrawn) The method of claim 53, wherein performing one or more tests includes at least:

performing one or more stress tests on said controller and said devices; and
if said one or more stress tests fail, performing one or more relaxed tests on said controller and said devices.

57. (Withdrawn) The method of claim 53, wherein performing said one or more tests includes at least:

driving a particular pattern on signals from said controller to said devices; and
checking whether portions of said particular pattern are accurately received by said devices.

58. (Withdrawn) A method comprising:

determining calibrated digital window centering values for registers of a controller by testing timing of signals between said controller and one or more devices,
wherein said registers affect said timing by affecting one or more of the following:
time delays introduced by first programmable delay cells directly into inputs of output buffers of said controller and time delays introduced by second programmable delay cells directly into outputs of input buffers of said controller.

59. (Withdrawn) The method of claim 58, wherein determining said calibrated digital window centering values is performed on a recurring basis.

60. (Withdrawn) The method of claim 58, wherein testing timing of said signals includes at least:

for each test value in a set of sequential test values:

setting a particular one of said registers to said test value;

driving a particular pattern on signals from said controller to said devices; and

checking whether portions of said particular pattern are accurately received by

said devices,

wherein the test value of said set closest to a median of test values of said set for

which said portions are accurately received is determined to be a calibrated

digital window centering value for said particular register.

61. (Withdrawn) An article comprising a storage medium having stored thereon instructions that, when executed by a computing platform, result in:

testing timing of signals between a controller and one or more devices for violations

of setup time restrictions and hold time restrictions of input channels of said

controller and said one or more devices by driving particular patterns on said

signals from said controller to said one or more devices and checking whether

portions of said particular pattern are accurately received by said one or more

devices.

62. (Withdrawn) The article of claim 61, wherein said instructions further result in:

repeating said testing a register of said controller set to a test value in a set of

sequential test values; and

programming said register with the test value of said set that is closest to a median of test values of said set for which said portions are accurately received.

63. (Withdrawn) The article of claim 62, wherein said register controls a time delay introduced by a programmable delay cell of said controller into an output signal of said controller.

64. (Withdrawn) The article of claim 62, wherein said register controls a time delay introduced by a programmable delay cell of said controller into an input signal of said controller.

65. (Currently Amended) The programmable delay cell of claim 1, ~~wherein the two or more pass gates comprise at least four pass gates~~ wherein the control signals are configurable to set at least eight different levels of combined impedance values.

66. (Currently Amended) The programmable delay cell of claim [[4]]1, wherein time delay of an input signal propagated via the programmable delay cell is controlled at least by changing the combined impedance ~~a first terminal of the variable impedance transistor is coupled to a high supply rail and a second terminal of the variable impedance transistor is coupled to only a source terminal of the switch transistor.~~